

INFORMATION SIGNAL RECORDING AND PLAYBACK METHOD
AND APPARATUS THEREFOR

1 BACKGROUND OF THE INVENTION

The present invention relates to a method and apparatus for recording and playing back PCM signals from a magnetic tape and more particularly to a
5 synchronization protecting apparatus well suited for recording and playing back a PCM sound when the overlap area of an 8 mm video tape recorder is expanded.

In the past, the track format 31 of the conventional 8 mm video tape recorder has been determined
10 as shown in Fig. 12. As shown in the Figure, a video signal 34 is recorded on an area 31 V corresponding to the cylinder head wrapping portion of 185 degrees and a PCM sound signal 37 time-base compressed to stereophonic sound data for one field is recorded on an area 31P
15 overlapping 36-degrees in the direction of the head scan entering side of the video signal 34. The 36-degree overlap area 31P includes a scan starting section 39 (a margin section for a head scan starting point), a preamble 38 (a clock regenerating signal for clock
20 pull-in purposes), the PCM sound signal 37, a postamble 36 (a margin section during the period of after recording) and a VP guard 35 (a guard section between the video signal and the PCM sound signal), and the PCM sound data 37 begins at the position of 5 degrees from the
25 head scan entering side. Then, the signals 38 to 36 are

1 subjected to biphase mark modulation and recorded on
the magnetic tape. With this PCM sound of the
conventional 8 mm video tape recorder, the sampling
frequency is 31.5 kHz and the number of quantization
5 bits is 10. These values are inferior in sound
quality as compared with the sampling frequencies of
48 kHz and 44.1 kHz and the number of quantization
bits or 16 bits which are the main trends in the field
of CD and DAT. However, since the PCM sound whose
10 sampling frequency is 48 kHz and whose number of
quantization bits is 16 has an amount of information
which is about three times that of the conventional PCM
sound, any attempt to realize such amount of information
in the same overlap area 31P of 36 degrees as previously
15 by utilizing the conventional PCM sound system requires
a line recording density of about 3 times the conven-
tional one.

Thus, the optimization of the correcting
codes has been effected to reduce the line recording
20 density and yet the line recording density of about 2.5
times has been required. And, in an attempt to realize
a high-density magnetic recording, a high-performance
tape has been used to optimize the modulation system
and yet it has been limited to the recording and
25 playback of the line recording density of about 2 times
that of the conventional PCM sound.

Therefore, in order that a PCM sound whose
sampling frequency is 48 kHz and number of quantization

1 bits is 16 may be realized in an 8 mm video tape recorder,
there is no alternative but to expand the overlap area
31P of 36 degrees. Fig. 12 shows a new 8 mm track
format 32 in which the overlap area is expanded by 5
5 degrees. By so expanding the overlap area 32P into a
linear audio track which is not used, it is possible
to realize a PCM sound having the sampling frequency
of 48 kHz and the number of quantization bits of 16 with
a line recording density of slightly over 2 times the
10 conventional one (see JP-A-1-119966).

By expanding the overlap area by 5 degrees,
it is possible to realize a sound having a sampling
frequency of 48 kHz and 16 quantization bits in terms
of line recording density. However, as shown in Fig.
15 12, expanding the overlap area by 5 degrees reduces the
distance from the lower edge of a magnetic tape 10 and
hence the head playback output at around the head entry
side of the track 32. This is due to the fact that upon
the entry of the cylinder head, the lower edge of the
20 magnetic tape 10 is turned up thereby increasing the
gap between the head and the tape. In this way, at
around the head entry side the S/N ratio is deteriorated
by the reduced playback output and hence the error rate
is deteriorated.

25 On the other hand, the vicinity of the head
entry side is also near to the head of PCM sound
data 42 and therefore a burst error tends to occur.
This is due to a synchronization error. The PCM sound

1 data 42 has a format 50 such as shown in Fig. 13 and
the sound data for one field is divided into several
blocks. Each block is added, as a header 51, with a
synchronizing signal, ID code (control signal), block
5 address and parity code as shown in Fig. 3 and they
serve important roles such as the synchronization for
converting serial signal data into parallel signal data
in terms of symbols and the generation of the accurate
RAM address for the sound data in the block. As a
10 result, a measure is taken so that during the period
of playback the synchronizing signal and the block
address in the header 51 are protected by referring to
the information preceding several blocks thereby
reducing the effect due to any desynchronization or
15 block address error. However, there is no information
to be referred to for the synchronizing signal and the
block address in the leading block and the protection
is deteriorated. More specifically, if an error is
caused in the header 51 of the leading block, during
20 the data conversion in terms of symbols a synchronization
error or RAM address error is caused thereby causing a
situation equivalent to the occurrence of a burst error
of the block length even if the sound data in the block
is correct entirely.

25 In this manner, the expansion of the overlap
by 5 degrees deteriorates the playback output at around
the head of the track as well as the error rate. Also,
the probability of a synchronization error or address

1 error in the leading block is increased and a burst error
of the block length tends to occur. As a result,
the probability of generating sound data by interpolation
is increased thus giving rise to a problem of deterioration
5 in the sound quality.

Disclosed in JP-A-60-247867 is a technique
for recording a synchronizing signal pattern in the area
of synchronizing clock signals for signal playback purposes
with a view to preventing such synchronization error in
10 the leading block of a track.

SUMMARY OF THE INVENTION

It is an object of the present invention to
provide means for protecting the synchronizing signal
and block address in a header of a leading block..

15 Here, let us note a preamble positioned in
the head entry side of PCM sound data. This preamble
signal is provided for the reason that a clock regenerat-
ing circuit requires a pull-in time of several tens
μs for the regeneration of the normal frequency from
20 the free running frequency and usually the minimum
recording wave length is recorded in order to increase
the edge component. However, even if the header
including the synchronizing signal, etc., is written in
the preamble, such information is subjected to the same
25 digital modulation as the data to manage the maximum
recording wave length and therefore no considerable
effect is caused on the pull-in time.

1 Thus, the above-mentioned object is accomplished
by writing the header information in the preamble to form
a dummy block structure.

By thus forming the preamble into a dummy
5 block structure including the headers, the dummy block
performs the same function as the leading data block of
the PCM sound data so that the leading data block of
the PCM sound data is enabled to refer to the synchroniz-
ing signals or the block addresses of the preceding
10 blocks so as to provide an effective protection.

In accordance with the present invention,
by virtue of the expanded overlap area there is an
effect that even if the playback output at around the
head scanning starting point is reduced so that the
15 error rate is deteriorated and an error is caused in the
header of the leading data block, it is possible to ensure
the protection of the synchronizing signal, the protection
of the block address and the generation of an address
thereby preventing the occurrence of a burst error of
20 a length corresponding to the block due to a synchroniza-
tion error or block address error in the leading
block.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B, 1C, 1D, 1E and 1F are diagrams
25 showing basic data arrangements according to an embodiment
of the present invention.

Figs. 2A and 2B are diagrams showing basic

1 data arrangements in a data frame according to the
embodiment of the invention.

Figs. 3, 4 and 5 show respectively the address
arrangements in data frames according to the embodiment
5 of the invention.

Fig. 6 is a basic block diagram of an embodi-
ment of a recording apparatus according to the invention.

Figs. 7A and 7B are flow charts showing
operations of the header generating circuit of Fig. 6.

10 Figs. 8A, 8B and 8C show examples of the
regenerating operations of a regenerating signal of a
digital information signal, with Fig. 8A showing an
arrangement of the digital information signal, 8B showing
a regenerating operation when the synchronizing signal
15 is detected being in error and 8C shwoing a regeneration
operation when the address is detected being in error.

Fig. 9 is a block diagram showing an embodi-
ment of a signal playback apparatus.

Fig. 10 is a block diagram showing a basic
20 operation of the synchronization protecting and
demodulating circuit of Fig. 9.

Fig. 11 is a block diagram showing an embodi-
ment of a recording and playback apparatus according to
the present invention.

25 Fig. 12 is a track format diagram showing
the track formats on a tape.

Fig. 13 is a diagram showing the data format
used in the embodiment of the present invention.

1 Fig. 14 is a diagram showing an arrangement
of the dummy block.

Fig. 15 is a data arrangement diagram showing
the content of the dummy block.

5 Fig. 16 is a modulated waveform diagram
showing the modulated waveform on the tape.

Fig. 17 is a block diagram showing the
operation of the synchronization protecting and demodulat-
ing circuit of Fig. 11.

10 DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of the present invention
will now be described. Figs. 1A, 1B, 1C, 1D, 1E and 1F
show the arrangements of data when the present invention
is applied to a digital information signal which is
15 transmitted or recorded in burst form. In Figs. 1A to
1E, symbol P designates preamble signals 1, D digital
signal data 2, H headers 3, S synchronizing signals 4,
A addresses 5, and PA parity codes 126. In the case
of a digital information signal which is transmitted
20 or recorded in burst form, a preamble signal for clock
regenerating purposes must be recorded in the portion
preceding the digital information signal in time.

The present invention notes the preamble signal
which is present before the digital information signal.
25 The digital information signal is usually formed into
a frame including a plurality of data blocks and a
header including a synchronizing signal, address, etc.,

1 is arranged at the head of each data block. The
synchronizing signal synchronizes the data block and
it also deals with desynchronization of the block,
etc. The address of the data block is written as the
5 address and it is utilized for the generation of an
RAM address during the period of signal processing. In
the arrangement of the digital signal, the header is
written in the data at intervals of a given time as
shown in Fig. 1A.

10 Consider now a case where an error is caused
in the header in Fig. 1 showing the conventional data
arrangement. Firstly, where an error is caused in any
other header than the leading header 3(a) or a header
3(b), for example, if the header 3(a) has been detected
15 and synchronization has been established, the
synchronous state can be maintained by utilizing the
fact that the headers are written at intervals of the
given time and also the value of the RAM address of the
header 3(b) can be accurately predicted due to the
20 fact that the address of the header 3(a) has been
read. However, where an error is caused in the leading
header 3(a), it is impossible to make a confirmative
determination as to the synchronous state to be referred
to or whether the error has been caused in the leading
25 header and hence it is impossible to predict the values
of the RAM addresses of the header 3(b) and the following.
As a result, the contents of the data become erroneous
until the accurate header is detected. Thus, as in the

1 case of Fig. 1B showing a data arrangement according
to the first embodiment of the present invention, if
headers 3 are written in a preamble signal 1 such that
they are synchronized with the headers in the data,
5 so far as any header in the preamble signal 1 has been
detected, it is possible to maintain the synchronous
state and accurately predict the values of the RAM
addresses even if an error is caused in the leading
header of the data. In the case of Fig. 1C where
10 synchronizing signals are written as headers, if synchro-
nization is established by the synchronizing signals in
the preamble signal 1, the data can be reproduced even
if the synchronizing signal is detected being in error.
In the case of fig. 1D where a synchronizing signal
15 and an address are written as each header, if values
which allow prediction of the value of the leading
address of the data are written as the addresses in
the preamble, not only an error in the synchronizing
signal can be dealt with but also the position of the
20 leading header 3(a) of the data blocks can be predicted.
In addition, the fact that the address 5 is written to
succeed the synchronizing signal 4 can be utilized such
that even if the same waveform as the synchronizing
signal is generated at a place other than the position
25 of the proper synchronizing signal in the preamble signal
during the regenerating operation, by determining for
example whether the waveform is accompanied with the
address signal, it is possible to determine whether the

1 waveform is the regular synchronizing signal.

Referring to Fig. 1E where an address parity code 126 is written, in addition to a synchronizing signal 4 and an address 5, as each header so that even
5 if the address is reproduced erroneously, the error in the address can be corrected by the parity check. The headers 3 can be written at intervals of a given time in a preamble 1, and in the embodiment of Fig. 1E they are written at a period which is two times the
10 data block length. The same modulation system as the data can be used on the headers in the preamble to manage the maximum recording wave length and thus no considerable effect is caused on the time for clock regeneration. It is to be noted that while the preamble signal for
15 PCM signal reproducing purposes includes generally a clock regenerating signal for clock regenerating purposes, in the case of regenerating for example a carrier-suppressed signal as in the S-VHS system, in order to regenerate the same carrier as the recording
20 side on the reproducing side, during the recording a carrier regenerating signal can be recorded along with a clock regenerating signal so as to insert the previously mentioned headers into these signals.

The second embodiment of the invention will
25 now be described. Fig. 2B is a diagram showing a data arrangement obtained when the present invention is applied to a digital information signal of the data frame structure such as shown in Fig. 2A which is

1 transmitted or recorded in burst form. Where the
digital signal data has the frame structure as shown
in Figs. 2A and 2B, a preamble 1 can be formed into a
block structure so that by recording a dummy header 7
5 of the same structure as the headers of a data frame 6
along with a dummy block 9 as shown in Fig. 2B, during
the reproduction the same effects as the previously
mentioned first embodiment can be obtained with respect
to the synchronization and the generation of RAM
10 addresses. Also, when protecting the synchronizing
signal and the address during the reproduction, the
dummy header 7 is the same in structure as the header
3 of the data frame 6 and therefore there is no need
to newly add any special protective method. Then,
15 as the value of the dummy data 8 in the dummy block 9,
data is written which makes a recording or transmitting
waveform advantageous for clock regeneration when using
the same modulation as the data frame 6.

Specific exemplary methods of designating block
20 addresses 11 of the dummy block 9 and the data blocks
will now be described. Figs. 3 to 5 show the methods
of designating the block addresses 11 of the dummy
block 9 when the leading address of the data blocks
is n . In the Figures, symbol S designates synchronizing
25 signals, I ID codes (control signals), BA block addresses,
P parity codes, DD dummy data and D data. In the case
of Fig. 3, the block addresses of the dummy block 9 are
respectively designated as $n-6$, $n-5$, $n-4$, $n-3$, --- with

1 respect to the leading address n of the data blocks,
so that if any one of the block addresses of the dummy
block 9 is reproduced as the accurate address, it
is possible to determine the number of blocks by which
5 this address precedes the leading address n so that
even if all of the following block addresses of the
dummy block cannot be reproduced, the position of the
leading address n of the data blocks can be predicted
accurately. Fig. 4 shows a case where addresses which
10 are not present in the block addresses 11 of the data
frame 6 are used as the block addresses of the dummy
block 9. This system has the advantage of easily
distinguishing the dummy block from the data blocks.

Fig. 5 shows an embodiment of the method
15 of designating the block addresses 11 which ensures
matching between the addresses and the control signals
when there are given relations therebetween. There
are cases where the control signals have different
control contents in relation with the addresses so
20 as to perform more complicated controls. For instance,
there is an instance where the control signal of a block
having an odd-numbered address performs a control
designated as "A" and the control signal of a block
having an even-numbered address performs a control
25 designated as "B". Thus, in the present embodiment,
if m represents the number of blocks in the data frame
6 and k the number of headers in the dummy block 9,
by designating the leading to the last block addresses

1 as $n+m-k$, $n+m-(k-1)$, --- $n+m-1$ or $n+m-(k-1)$, $n+m-(k-2)$,
---, $n+m$, the previously mentioned matching between
the addresses and the control signals can be ensured.

In this way, by using as the block addresses
5 of the dummy block 9 such values capable of predicting
the value of the leading address n of the data blocks
in the data frame 6 in accordance with a certain
rule, it is possible to generate an accurate address
even if an error is caused in the header of the leading
10 data block.

The third embodiment of the invention will
now be described. Fig. 6 is a basic block diagram
of an embodiment of a recording apparatus for recording
a digital information signal on a magnetic tape in
15 accordance with the present invention. The digital
information signal applied to a data input terminal 201
is applied to a signal processing circuit 202. The
signal processing circuit 202 performs interleaving of
the data, the generation and addition of error correct-
20 ing codes, etc., and data generating circuit 203 generates
data which is modulated into a clock regenerating signal
after the modulation. The outputs of the signal
processing circuit 202 and the data generating circuit
203 are applied to a data selector circuit 204 so that
25 the input from the data generating circuit 203 is selected
and generated during the interval of the clock regenerat-
ing signal and the input from the signal processing
circuit 202 is selected and generated during the interval

1 of the digital information signal. A header generating
circuit 205 generates synchronizing signals, addresses,
control signals and error detecting signals. As
regards the method of designation used in the generation
5 of addresses, where the designation of addresses is
to be effected as for example in the case of the
embodiment of Fig. 3, if n represents the leading
address, the addresses are designated in time sequence
as n , $n+1$, $n+2$, --- in the interval for recording the
10 digital information signal, whereas in the interval
for recording the clock regenerating signal, the
generation of addresses is effected in the form of
 $n-k$, ---, $n-2$, $n-1$ if the number of blocks in the clock
regenerating signal interval is represented by k .
15 These operations will be described in greater
detail in reference to the flow charts of Figs. 7A and
7B. The number of symbols in each data block is S
(block 230). The first generated address value $n-k$
is produced first (processing block 231). A processing
20 block 232 generates a header including an address
formed by the generated address, a control signal
formed by control data and an error detecting signal
(parity check) formed by logically combining the
address and the control signal. Then, a decision block
25 233 makes a decision on the address so that a transfer
is made to a processing block 234 where clock regenerat-
ing data is added to the header (when address $< n$ is YES)
and a transfer is made to a processing block 235 where

1 PCM data is added to the header (when address < n is NO).

Each header is formed by a total of four symbols (S-4), that is, it is formed by a synchronizing
5 signal (which is added by a processing block 236 described later), a control signal, an address and a parity check which are each formed by a single symbol, and the processing block 234 adds to the S-4 symbols data which is useful for clock regenerating purposes (i.e.,
10 data which results in a clock regenerating signal after modulation). Similarly, the processing block 235 adds the PCM data and an error correcting code to the S-4 symbols. Finally, the processing block 236 adds a synchronizing signal as mentioned previously thereby
15 completing one data block and the data block is modulated and recorded on a magnetic tape (processing block 237).

Thus, 1 is added to the address value of the data block (processing block 238) to generate the next
20 address, and thereafter the similar processing is repeated.

The operation of recording a carrier suppressed signal as in the case of the previously mentioned S-VHS system will now be described with reference to Fig. 7B.
25 The operation differs from the processing of Fig. 7A in that a synchronizing signal is added in the generation of a header (processing block 250) and that data useful for carrier regeneration and clock regeneration

1 are added by a processing block 251. The data useful
for carrier regeneration and clock regeneration may be
such data having a wavelength which is two times the
minimum recording wave length. Also, it is possible to
5 add the carrier regenerating signal to the front block
and add the clock regenerating signal to the rear
block.

The other processing operations of Fig. 7B
are practically the same as Fig. 7A, and a completed
10 data block is carrier modulated (processing block 252)
and recorded.

The output of the header generating circuit
205, which generates the header by the above-mentioned
operation, and the output of the data selector circuit
15 204 are applied to another selector circuit 206 which
in turn changes its positions at intervals of one
data block period irrespective of the interval of the
clock regenerating signal (the signal from the data
generating circuit) and the interval of the digital
20 information signal. The output of the selector circuit
206 is modulated by a modulator circuit 207 so that the
data from the data generating circuit 203 is modulated
to a clock regenerating signal. The signal modulated
by the modulator circuit 207 is applied to a recording
25 circuit 208 so that the signal is written on the magnetic
tape thereby writing in the clock regenerating signal
the headers of the same structure as the headers in
the digital information signal so as to be synchronized

1 with the latter headers.

 An example of a reproducing method according to the present invention will now be described as the fourth embodiment. Figs. 8A, 8B and 8C show examples
5 of an operation performed when the invention is applied to the reproduction of a digital information signal. Fig. 8B shows an operation performed when the first synchronizing signal of the digital information signal is in error. Since the synchronizing signal is
10 reproduced at a given period as shown in the Figure, if only the single accurate synchronizing signal is reproduced in the clock regenerating signal interval, due to the reproducing period of the synchronizing signals being known preliminarily, by using a synchronous
15 counter which repeats at the period of the synchronizing signals as shown in the Figure, the positions of the synchronizing signals can be detected in accordance with the count values of the synchronous counter. As a result, even if the leading synchronizing signal
20 of the digital information signal is detected in error, the data can be reproduced accurately. At this time, the determination of whether the synchronizing signal is accurate or not is made in such a manner that the control signal (ID code), the address and the error
25 detecting signal (parity code) immediately following the detected synchronizing signal are calculated and the determination is made on the basis of non-existence of error. Fig. 8C shows an operation performed when the

1 first address of the digital information signal is in
error. If at least one accurate address is reproduced
in the clock regenerating signal interval as shown in
the Figure, due to the fact that the reproduction period
5 of the synchronizing signals is known, even if an error
is caused in the following addresses, the address value
can be counted up at the given period so that the
accurate addresses can be generated even though the first
address of the digital information signal is in error.
10 At this time, the determination of whether the address
is accurate or not is made in the same manner as in
the case of Fig. 8B, that is, the control signal, the
address and the error detecting signal are calculated
and the determination is made on the basis of the non-
15 existence of error and the continuity of the reproduced
address.

By using the above-mentioned reproducing
system, even if the first synchronizing signal of the
digital information signal is in error, synchronization
20 can be maintained starting from the first data of the
digital information signal. Also, even if the first
address of the digital information signal is in
error, by detecting the accurate address in the clock
regenerating signal interval, it is possible to generate
25 the accurate address starting at the first data of the
digital information signal.

The fifth embodiment of the invention will now
be described. Fig. 9 is a basic block diagram in which

1 the present invention is applied to the reproduction
of a signal including a clock regenerating signal and
a digital information signal which are divided in
area. The reproduced signal applied to a reproduced
5 signal input terminal 210 is subjected to signal
amplification and clock regeneration by a regenerating
circuit 211 and the resulting digital waveform is applied
to a synchronization protecting and modulating circuit
212. The synchronization protecting and modulating
10 circuit 212 performs the following processing. Fig. 10
is a block diagram showing a basic operation of the
synchronization protecting and modulating circuit 212.
The input reproduced signal is applied to a synchronizing
signal detecting and protecting circuit 218 so that the
15 data synchronizing signal is detected starting from the
clock regenerating signal interval and the detected
synchronizing signal is checked as to whether it is
accurate. If it is determined accurate, the synchronous
counter is initialized and the counting is repeated at
20 the reproduction period of the synchronizing signals,
thereby maintaining the accurate synchronization.
On the contrary, if it is determined inaccurate and
there is no preceding accurate synchronizing signal,
the detection of the synchronizing signals is always
25 effected. By thus performing a data synchronizing
operation starting from the clock regenerative signal
interval, it is possible to maintain the synchronization
of the data even if the first synchronizing signal of the

1 digital information signal is in error. The data
synchronized by a synchronizing circuit 219 is de-
modulated by a demodulator circuit 220 to produce
digital data. Then, the addresses are detected from
5 the demodulated digital data by an address detecting
and protecting circuit 221. The detection of the
addresses is also started from the clock regenerating
signal interval and a decision is made as to whether
the detected address is accurate. If it is determined
10 accurate, the address is maintained. If it is
determined inaccurate, an accurate address is generated
by using the previously maintained address. By thus
performing the address protecting operation starting
from the clock regenerating signal interval, it is
15 possible to maintain the proper time sequential order
of the data even if the first address of the digital
information signal is in error. The addresses generated
by the address detecting and protecting circuit 221
are applied to a clock regenerating signal discriminat-
20 ing circuit 213 of Fig. 9 so that the clock regenerating
signal and the digital information signal are discriminated
from each other and the clock regenerating signal is
deleted by a clock regenerating signal eliminating
circuit 214. After the clock regenerating signal has
25 been eliminated, the digital information signal is
applied to a signal processing circuit 215 which performs
an error correcting process and data interleaving thereby
reproducing it as the digital information signal.

1 By thus effecting the protection of the
synchronizing signals and the addresses starting from
the interval of the clock regenerating signal during
the reproduction, it is possible to prevent the occur-
5 rence of a burst error at around the top of the digital
information signal due to the inaccurate first synchro-
nizing signal or address of the digital information
signal.

 The sixth embodiment of the invention will
10 now be described. Fig. 11 is a basic block diagram
of this embodiment in which the invention is applied
to an apparatus for recording a digital information
signal in burst form on a magnetic tape and reproducing
it, e.g., the PCM sound of an 8 mm video tape recorder.

15 The operation of the recording system will be
described first. The analog signal applied through
an analog signal sound input terminal 101 is quantized
at a given sampling frequency by an A/D converter 102
thereby converting it to digital signal data in terms
20 of quantization bits. Data in terms of symbols is
generated from the converted digital signal data by
a symbol generating circuit 103 and a signal processing
circuit 104 generates correcting codes, headers, etc.,
from the symbol data, thereby producing a format 50
25 such as shown in Fig. 13. In the case of the format
shown in Fig. 13, the field frequency of video signal
is selected 60/1.001 Hz according to the NTSC and it
corresponds to the sound data for one field. While the

1 format of this embodiment will be described on the basis
of the NTSC system, the present invention is suitably
applicable to any other system such as the PAL system.

The structure of the format 50 includes an
5 array of 110 blocks each including 44 symbols, and a
header 51 is provided with a synchronizing signal,
ID code (control signal), block address and parity code
resulting from an exclusive OR operation on the ID
code and the block address. Each block is provided
10 with a 4-symbol C_1 code 52, and a single 4-symbol C_2
code is added to each C_2 code system with an interleave
of 5 blocks as shown in Fig. 13 thereby adding a
total of 20 blocks of C_2 codes 53.

With the format shown in Fig. 13, the data frame
15 50 is provided with a dummy block 60 by a dummy block
adding circuit 105 so as to be placed in a position on
the head entry side as shown in Fig. 14. As shown in
Fig. 14, the dummy block 60 is provided with dummy
headers 61 and each dummy header 61 is provided with a
20 synchronizing signal, ID code (control signal), block
address and parity code as in the case of the data block
header 51. Fig. 15 shows the header portion in an
expanded form. In the Figure, designated by SYNC are
synchronizing signals, ID ID codes, B.Adr block addresses,
25 and PARITY parity codes. The block addresses of the
dummy block 60 represent an application of the previously
mentioned embodiment shown in Figs. 3 and 4. At this
time, the synchronizing signal is replaced by a modulated

1 code of "311" (sexadecimal) or "111" (sexadecimal) by
a modulator circuit 106 in correspondence to the
preceding modulation pattern. Fig. 16 shows the modu-
lated waveform generated when the leading block of the
5 dummy block is actually recorded on the tape. The
modulated waveform is obtained by first converting
the data to a modulated code, converting the modulated
code to a serial data and then subjecting the serial
data to NRZI conversion.

10 By forming the data 62 in the dummy block
into "EB" (sexadecimal), it is converted to "1111111111"
(binary) in terms of an 8-10 modulated code (see
DIGITAL AUDIO TAPE RECORDER SYSTEM DAT JUNE 1987
THE DAT Conference, PP. 32, 38).

15 By performing the NRZI conversion, it is
possible to produce a continuous modulated waveform
of the minimum recording wave length by the output of
the modulator circuit 106.

In accordance with this embodiment, due to the
20 use of the 8-10 modulated code, the modulated waveforms
of the other data can be limited to a wavelength which
is 4 times the minimum recording wave length at the
most (i.e., the modulated waveform of sync) and there
is practically no effect on the pull-in time during
25 the clock regeneration.

After the dummy block 60 of Fig. 14 has been
added in this way, the data frame 50 is modulated by the
modulator circuit 106 and it is then applied to a

1 recording circuit 107. In this case, the video signal
applied through a video input terminal 12 is also
processed by a recording video signal processing circuit
108 thereby applying it to the recording circuit 107.
5 The recording circuit 107 distributes the PCM signal
and the video signal to the two heads of a cylinder
109 thereby recording the signals on a magnetic tape 110
in the form of a new 8 mm track format 32 of Fig. 12
in which the overlap area is expanded by 5 degrees
10 as compared with the previously mentioned conventional
PCM signal.

Next, the operation of the playback system
will be described. The magnetic record pattern on the
magnetic tape 110 is detected by the two heads of
15 the cylinder 109 and the reproduced signal is applied
to a playback circuit 111. The playback circuit 111
amplifies and divides the signal into the PCM signal
and the video signal according to the recording areas
so that the video signal is applied to a reproduced video
20 signal processing circuit 112 and the PCM signal is
subjected to clock regeneration thereby applying the
signal as serial digital signal data, along with the
regenerative clocks, to a synchronization protecting and
modulating circuit 113. The synchronization protecting
25 and modulating circuit 113 performs the protection
and demodulation of the synchronizing signals and the
blocks addresses. Fig. 17 is a block diagram showing the
overall operation of the synchronization protecting

1 and demodulating circuit 113 and a dummy block eliminat-
ing circuit 114 and the operation will now be described.

The reproduced data and the regenerated clocks
are applied to a shift register 80 which converts the
5 input data to a parallel signal and a synchronizing
signal detecting circuit 82 detects the synchronizing
signals. After the synchronizing signals have been
detected, the detected signals are applied to a synchro-
nous counter 83 through a detection window generating
10 circuit 84 thereby providing synchronization in terms
of symbols. A demodulating and synchronizing circuit
81 effects the synchronization and demodulation in
terms of symbols. In this case, the protection of the
synchronizing signals is effected by a synchronization
15 and address protecting circuit 90 and the detection
window generating circuit 84. The basic operation
utilizes the fact that the synchronizing signals are
reproduced at the rate of one for every block at
intervals of the given time. In other words, after
20 the regular synchronizing signal has been detected for
the first time, the synchronizing signals are detected
only for the detection window at intervals of a certain
time, whereas when the regular synchronizing signal
is not detected, the protection of synchronization (the
25 maintenance of the preceding synchronous state) is
effected for the interval of the several blocks. There-
after, if any synchronizing signal is not detected,
a search is made again for the regular synchronizing

1 signal. In this case, the normality of the synchronizing
signal is determined in accordance with the normality
of the block address. By effecting the synchronization
protection by such procedure, errors in the synchronizing
5 signals and demodulation of the reproduced signal can
be dealt with. The thus synchronized symbol data is
written in an RAM 93 through a data bus 94.

The protection of the addresses during the
writing into the RAM 93 will now be described. The
10 block addresses correspond to the addresses in the RAM
93 and thus if any error is caused in the addresses so
that the data is written at the inaccurate RAM address,
the time sequential order of the reproduced signal is
deranged and it leads to inaccuracy of the blocks on
15 the whole. Therefore, the protection of the addresses
must be effected effectively. In the apparatus of the
embodiment shown in Fig. 17, the normality of the
addresses is determined in such a manner that the
provision of protection is determined in accordance
20 with the results of ① a parity check circuit 87 for
checking the parity of the header 51, ② an address
continuity check circuit 88 and ③ a reproduced address
≤ decoded address check circuit 89. In other words,
only those addresses which have passed the above checks
25 ① to ③ are determined as being accurate and the
reproduced addresses are used as the RAM addresses.
If the reproduced address is in error so that the address
fails to pass these checks ① to ③, the address

1 protection is performed and the count value from the
accurate address preceding the occurrence of the
inaccurate reproduced address is used as the RAM
address.

5 By providing such address protection, it is
possible to generate a highly reliable RAM addresses
even if any block address, ID code (control signal)
or parity code of the header is detected as being in
error.

10 Let us consider for purposes of comparison
the reproduction of the conventional data format
which has not been provided with the dummy block.
Consider first a case where during the synchronization
the synchronizing signal of the leading block is in
15 error so that the synchronizing signal cannot be detected
by the synchronizing signal detecting circuit 82. In
this case, since the error is in the leading block so
that there is no synchronization to be referred to,
no synchronization protection can be provided. Thus,
20 the synchronization in terms of symbols cannot be
provided so that all the data are in error until
the normal synchronizing signal is detected next.

Next, considering a case where the block
address of the leading block is in error, then there
25 exists no accurate address preceding the occurrence
of the error and thus the protection cannot be effected.
Also, it is impossible to show the number of this block
in the sequence. As a result, the whole block is

1 considered to be in error and a "0" is written in the
address of the RAM 93.

Thus, where errors are caused in the header
of the leading block, it is difficult to protect the
5 leading synchronizing signal and the leading block
address and the provided protection, if any, will be
less effective one using an area signal or the like.
However, by adding the dummy block 60 shown in Fig. 14
to the data frame 50 as in the embodiment of the present
10 invention, although the leading synchronizing signal
of the data block is in error, if the normal synchroniz-
ing signal can be detected during the reproduction of the
several blocks of the dummy block 60, there is no danger
of causing a burst error of a length corresponding to
15 the block due to the synchronization error in the
leading data block.

It is to be noted that even if the leading
synchronizing signal of the dummy headers 61 is in
error, this only causes the leading block of the dummy
20 block 60 to be in error.

Also, where the leading address of the data
blocks is in error, by designating the block addresses
in the headers of the dummy block as shown in Fig. 5
so as to permit the prediction of the position of the
25 leading data block, the data of this block can be
written in the accurate address of the RAM 93. Also,
although the leading address and the block address
of the dummy block are simultaneously in error, if

1 the normal block address is detected during the reproduc-
tion of the several blocks of the dummy block 60, in
accordance with the time-like count value from the
detected block address the address protection can be
5 effected even if an address error is caused in the
leading data block and the data block can similarly
be written in the accurate address of the RAM 93. It
is to be noted that even if the address error is caused
in the dummy block as mentioned above, this portion is
10 a dummy and therefore no inconvenience is caused.

It is to be noted that where the accurate
block address is detected from the dummy block, while
a processing is required such that the dummy data of
the dummy block is not written in the RAM 93, the
15 block address of the dummy block has a value which
does not exist in the addresses of the data blocks and
therefore it can be easily discriminated by a dummy block
discriminating circuit 86. Also, even if the dummy
data is written in the RAM 93, it is only necessary
20 to perform a signal processing such that the RAM ad-
dress in question is not used. Also, the control infor-
mation corresponding to the control signals (ID codes)
of the data frame are written in the control signals
(ID codes) of the dummy block according to the block
25 addresses.

Let us now consider the reproduction of PCM
sound from an 8 mm video tape recorder which records
and plays back the previously mentioned, 16-bit PCM

1 sound. Where the conventional data frame provided
with no dummy block 60 such as shown in Fig. 13 is
reproduced, burst errors of the block length are
caused until the normal synchronizing signal is next
5 detected from the leading data block as mentioned
previously. Thus, since the top of the PCM sound data
42 comes closer to the lower edge of the tape due to
the expansion of the overlap area as shown in Fig. 12,
when the cylinder heads 9 come in, the tape 10 is turned
10 up thereby reducing the reproduced output due to the
effect of the increased gap between the tape 10 and the
heads 9. As a result, the error rate is deteriorated
at around the head of the PCM sound data 42 and this
increases the probability of failing to detect the
15 synchronizing signal of the leading data block. There-
fore, the probability of causing a burst error of the
block length from the leading data block is increased
and hence the probability of generating the sound by
interpolation of the data is increased, thus causing
20 deterioration of the sound quality.

Therefore, the dummy block 60 is added to the
data frame 50 in the previously mentioned manner.

By applying the method and apparatus of the
present embodiment to a 8 mm video tape recorder which
25 records and reproduces such PCM sound, even if errors
are caused in the leading data block during the sound
reproduction, it is possible to provide protection
for the synchronizing signal and the block address

1 thereby reducing the probability of causing a burst
error of the block length due to a synchronization
error or RAM address error. In other words, when
a synchronization error or RAM address error is caused
5 in the leading data block of the data frame provided
with the dummy block, this means a case where errors
are caused in all the headers 61 of the dummy block
60 and its probability is extremely small.

In this way, the data written in the RAM 93
10 is subjected to error detection and processing of the
ID codes (control signals) by a signal processing
circuit 115 and a symbol composing circuit 116 composes
word data of a given number of quantization bits from
the symbol data. Then, a D/A converter 117 converts
15 the digital signal data to analog signal data and a
sound signal is generated from a sound output terminal
118.

While the embodiments of the recording and
playback apparatus according to the invention have
20 been described as applied to an 8 mm video tape recorder
with PCM sound to show its effects, the recording and
playback apparatus of this invention is not limited
to the 8 mm video tape recorder and it is suitably
applicable to apparatus of the type employing cylinder
25 heads to record a digital signal in burst form on a
magnetic recording medium, such as, a video tape recorder
and other apparatus for recording and reproducing video
signals and PCM sound signals, apparatus for recording

1 video signals themselves in PCM form, and apparatus
for recording only sound signals in PCM form such as
a DAT.